Office Action Summary	Application No.	Applicant(s)	
	10/673,507	STRANG, ERIC J.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 26 August 2010.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7,9-11,14-48,51-74 and 78-80 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7,9-11,14-48,51-74 and 78-80 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 20100905 .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-7,9-11,14-48,51-74 and 78-80 has/have been presented for examination based on amendment filed on 08/26/2010.
2. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 08/26/2010 has been entered.
3. Claim(s) 1, 38 and 78 is/are amended.
4. Claim(s) 1-7,9-11,14-48,51-74 and 78-80 remain rejected under 35 USC § 112.
5. Claims 1-7, 9-11, 14-21, 29-30, 32-34, 37, 79 and 38-48, 51-58, 66-67, 69-71, 74, 80 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view of **Tan**.
6. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of I Yunemura.
7. Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view of **Tan**, further in view of **Chen**.

8. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of N**ikoonahad**.

9. Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Sonderman**, in view of **Jain**, further in view **Tan**, further in view of **Fatke**.

10. This action is made Non-Final.

Claim Interpretation

Claim 1 discloses "spatially resolved model", however the disclosure appears to lack a definition what a spatially resolved model (See specification: [0037] [0098]) constitutes to gain better understanding of the claim. Further claim appears to indicate the have "spatially resolved model" as intended use of the "first principles simulation model" as in:

> "solving the computer-encoded differential equations of the first principles simulation model for the spatially resolved model in a time frame shorter in time than the actual process being performed;…"

Therefore no patentable weight is given to "spatially resolved model". Further if applicant intends to recite more positively the "spatially resolved model", two things are needed. First, a clear definition of the spatially resolved model with support from specification; Second, a recitation of connection to "first principles simulation model" (e.g. a type of "first principles simulation model") and how it meets the shorter time frame requirement for concurrent execution with the wafer process.

Response to Applicant's Affidavit

The Declaration under 37 CFR 1.132 filed 8/26/2010 is insufficient to overcome the rejection of the claims based upon the prior art rejections as set forth in the last Office action because:

a. As per Item #2: In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Further applicant has presented mere allegation without evidence in "2)" and "3)".

b. As per Item #3: "*Applicant has not provided any evidence of lack of reasonable expectation of success*. MPEP 2143.02 states: Obviousness does not require absolute predictability, however, at least some degree of predictability is required. <u>Evidence showing there was no reasonable expectation of success may support a conclusion of nonobviousness</u>. In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976).

c. As per Item #4: Applicant has provided no evidence, furthermore, the relevance to the fact pattern is unclear.

d. As per Item #5: In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of

references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Further applicant's statement is conclusory.

e. As per Item #6: Applicant's statement is speculative; no facts are provided to support the rationale. Furthermore, in assessing the probative value of an expert opinion, the examiner must consider the nature of the matter sought to be established, the strength of any opposing evidence, the interest of the expert in the outcome of the case, and the presence or absence of factual support for the expert's opinion. (MPEP 716.01(c) III). In this case, the inventor is acting as expert.

Response to Applicant's Remarks for 35 U.S.C. § 103

(Argument 1) Applicant has argued in Remarks Pg.20:

> Thus, the Board's decision rests on a presumption that Tan et al use actual process parameters for an actual process to complete a simulation **[1]**.
>
> Yet, this position is not supported by Tan et al. Tan et al describe at col. 2, lines 7-10, model-based real time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run. Yet, a "model-based" real time process control does not specify when the model is completed, **[2]** only that the "process control" in Tan is real time.

(Response 1) As per **[1] & [2],** The Examiner has no jurisdiction over issues decided by the board and makes no additional comment.

(Argument 2) Applicant has argued in Remarks Pg.23:

> Tan et al do not disclose or suggest solving computer-encoded differential equations of the first principles simulation model for a spatially resolved model of a physical geometry of the semiconductor processing tool in a time frame shorter in time than the actual process being performed.

(Response 2) In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case Sonderman and Jain is used to show the argued limitation.

(Argument 3) Applicant has argued in Remarks Pg.23:

> Applicants' position on this matter is supported by the fact that Tan et al teach the use on an existing process model for feedback or feed forward processing. <u>In feedback control, by definition, the results of a process step are provided to a subsequent wafer.</u> **<u>In the feed forward control of Tan et al, the results of a prior process step are used to adjust a subsequent process being run of the wafer.</u> [2]** Indeed, as noted below, the metrology machine 206 of Tan et al measures post-process data, and **<u>by definition could then not set initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool based on the input data for the actual process being performed by the semiconductor processing tool.</u> [1]** Tan et al describe:
>
> …
> Thus, Tan et al use post-process data to **update and store [3]** a model for a subsequent processing step. It is the updated model (based on data measured from a prior run) that is used to control the next process run, thereby providing model-based real time process control during the process run where the model is based on data from a previous run producing an updated and stored simulation result for process control.
>
> In other words, in Tan et al, <u>the solution to model exists from previous runs</u>, and essentially the whole detailed description of Tan et al revolves around the issue of how one can keep these models up-to-date as wafers are processed. Figure 2 of Tan et al (reproduced below) shows explicitly the use of "feed-forward data" and "feed-back data" for process control modifications. **Figure 3 of Tan et al shows explicitly the use of"pre-process metrology" in what would be a feed-forward control scheme. [4]** Figures 4 and 5 describe the use of an updated model to control a subsequent process.

(Response 3) As per **[1],** The Examiner has no jurisdiction over issues decided by the board and makes no additional comment.

Further, On the contrary (to [2]) applicant specification discloses and relies upon the feed forward controls.

> [0057] … The first principles simulation may also be run concurrently without the use of physical sensor input data. In this embodiment, initial and boundary conditions for the simulation are set

> based on the initial setting of the tool prior to a tool process and the readings of physical sensors prior to the run; a full time-dependent simulation is then run during, but independent of, the tool process. The obtained virtual measurements can be displayed-to and analyzed by the operator like any other actually measured tool parameter. If the simulation runs faster than the wafer process, then simulation results are known ahead of the corresponding actual measurements made during the wafer process. Knowing the measurements ahead of time allows the implementation of various **feed-forward control functions** based on these measurements as will be further described below.

Further as per [3], allegation that relating to update and store of the model does not negate the fact that in situ data is used as input to the model (e.g. from Tan Fig.2 Metrology machine #1 *204*). There is no requirement in claim that the model cannot be updated in subsequent simulation runs. Further even in Sonderman it is made clear that the model and model input are separate (Sonderman: Col.7 Lines 8-20). Further as per [4], see the applicant's own specification [0057] using feedforward data and response for [3].

(Argument 4) Applicant has argued in Remarks Pg. 25:

> In short, Applicants submit that they were the first to technically realize a way to solve computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a semiconductor processing tool in a time frame shorter in time **[1]** than the actual process being performed in the semiconductor processing tool.
>
> The attached declaration by Andrej Mitrovic, one of the named inventors, attests to the fact that neither Sonderman et al nor Tan et al use a first principles simulation model. Rather, the models in these references are 1) simplified models based on former approximate solutions or 2) statistical or "learned" models tracking how the systems are expected to behave.

(Response 4) As per [1], Applicant's specification does not disclose *how* the applicant is first to technically realize a way to solve computer-encoded differential equations of a first principles simulation model for a spatially resolved model of a semiconductor processing tool in a time frame shorter in time as argued. Furthermore, applicant's affidavit provides no evidence. Since, Jain (1994) and applicant's alleged reduction to technically realize the invention (~2002) computing capacity has nearly doubled every two years (Moore's Law), therefore one of the ordinary skill in the art in 2002 would not see the

teaching of Jain as futuristic. Applicant has provided no evidence to the contrary, of this disclosure so futuristic that it cannot be made or used and further that evidence of 2002 technically realizing this invention.

(Argument 5) Applicant has argued in Remarks Pg.27-29:

> Support for Applicants position is found in the following three references 1) U.S. Pat. No. 6,185,472; 2) U.S. Pat. No. 7,047,095; and 3) U.S. Pat. No. 6,587,744.

(Response 5) Applicant has cited art which is not of record (cited on PTO 892) and not used to reject the claims. Applicant's showing that other patents still teach longer simulation times as compared to wafer processing time, does not alleviate the fact that the applicant's disclosure seems to be silent on **how** ***"spatially resolved model*** *of a semiconductor processing tool could have been solved in a* ***time frame shorter*** *in time than the actual process being performed in the semiconductor processing tool".*

Citation of Inventor's affidavit on remarks 29 is still not evidence (e.g. publication, notes copy etc.) that such compression was achieved. Further, the methodology used to achieve this compression in time is not part of the specification and would be *essential subject matter* to enable the invention.

(Argument 6) Applicant has argued in Remarks Pg.29-31:

> Once again, Appellant sees no disclosure in Chen of:
>
> calculating a solution to the first principles simulation by applying a close-fitting solution to thereby set initial conditions for cells in the first principles simulation.
>
> Rather, the attached declaration attests to the fact that this section of Chen is directed to the arithmetic manipulation of input data, and is not directed to any kind of solution, much less a "close-fitting solution," to a first principles simulation, as defined in Claims 23-26 and 60-63.

(Response 6) Applicant has cited the section mapped by examiner Specifically Chen Col.5 Lines 38-67 discloses a fitting function mapped to close fitting solution. For at least the above reasons applicant's argument's and affidavit is found to be unpersuasive.

Referring to FIGS. 3A and 3B, two-run process of the simulation system 200 includes two different run modes of operation, specifically a calibration run 310 depicted in FIG. 3A, and a prediction run 320. In the calibration run 310 depicted in FIG. 3A, available data are processed to generate fitting functions for matching simulated and measured data. The calibration run 310 includes a single simulation step 312 and actual measurements 314. Results of the simulation step 312 and the actual measurements 314 are processed according to a fitting function 316. The calibration run 310 includes a series of single simulation steps 312, each with corresponding actual measurements (both process parameters and in-line/WET data) 314. Results of a plurality of the simulation steps 312 and the actual measurements 314 are processed to produce a fitting function 316. Each simulation step 312 processes data accumulated using all fitting functions previously calculated during the calibration run 310.

In the prediction run 320 depicted in FIG. 3B, measured data and the fitting functions calculated in the calibration run 310 are used to predict unknown data. During the prediction run 320, if any process parameter is missing from the existing database, the statistical distribution function used in the corresponding calibration run 310 replaces the missing parameter. If any WET data or in-line parameter is contained in the existing dataset, these WET data or in-line parameters replace computed values without changing fitting functions.

Referring to FIG. 4, a flow chart of a calibration process 400 of the statistical simulation method is shown. The calibration process 400 includes two parallel processes including an actual in-line process 420 and a simulation

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Claim Rejections - 35 USC § 112¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. Claims *1-7,9-11,14-48,51-74 and 78-80* are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for *setting initial and boundary condition for first principle physical model*, does not reasonably provide enablement for *setting initial and boundary condition for a spatially resolved model of physical geometry of the semiconductor processing tool* as claimed in claim 1, 38 & 78. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. Applicant's disclosure in [0035] stating "physical model may include a spatially resolved model of the physical geometry of the tool" is not sufficient to meet the enablement requirement as applicant themselves admitted in [0035] that each model for CVD different from furnace. Dependent claims 2-7,9-11,14-37 & 39-48,51-74 and 79-80 are rejected as inheriting this deficiency respectively from claims 1 & 38.

12. Claims *1-7,9-11,14-48,51-74 and 78-80* are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for solving the computer-encoded differential equations of the first principles simulation model in a time frame shorter in time than the actual process being performed (Specification: [0056] [0057]), does not reasonably provide enablement for *solving the computer-encoded*

differential equations of the first principles simulation ***model for the spatially resolved model*** *in a time frame shorter in time than the actual process being performed*. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the invention commensurate in scope with these claims. The spatially resolved model (Specification: [0035]) is a type of model for a physical tool and is different for each tool as disclosed in the specification. Applicant has also shown that some simulation for the first principle model cannot be run concurrently with the wafer process and may take longer. There is no disclosure that this specific type of model (i.e. "spatially resolved model") can be run concurrently *in a time frame shorter in time than the actual [wafer] process being performed*. Dependent claims 2-7,9-11,14-37 & 39-48,51-74 and 79-80 are rejected as inheriting this deficiency respectively from claims 1 & 38.

13. Claim *1-7,9-11,14-48,51-74 and 78-80* are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what spatially resolved model as an example of first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling, although they rely on the commercially available packages to model the various first principle simulation models, the details of the spatially

resolved model are absent from the specification. The details of these model which lead to unexpected results are very relevant to the designing the first principle physical model. Dependent claims 2-7,9-11,14-37 & 39-48,51-74 and 79-80 are rejected as inheriting this deficiency respectively from claims 1 & 38.

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claims <u>1-7, 9-11, 14-21, 29-30, 32-34, 37, 79</u> and <u>38-48, 51-58, 66-67, 69-71, 74, 80</u> and <u>78</u> are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (<u>Sonderman</u> hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (<u>Jain</u> hereafter) further in view U.S. Patent No. 6,263,255 issued to Tan et al (<u>Tan</u> hereafter).

<u>Regarding Claim 1 (Updated 9/3/2010)</u>

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (**Sonderman**: Summary, at least in Col.2 Lines 10-17; Col.3 Lines 45-49) by ***inputting*** *a inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool* (**Sonderman**: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model.

Further, **Sonderman** teaches ***inputting*** *process data relating to an actual process being performed by the semiconductor-processing tool* (**Sonderman**: at least in Col.3 Lines 50-67; *Col.7 Lines 8-20*).

Further, **Sonderman** teaches ***based*** *on the input data for the actual process being performed by the semiconductor processing tool* (**Sonderman**: Col.7 Lines 7-20), *setting initial and boundary conditions for a spatially resolved model of a physical geometry of the semiconductor processing tool* (**Sonderman**: Col.7 Lines 21-35) as predetermined specifications.

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches ***solving*** *the computer-encoded differential equations of the first principles simulation model* using MPE engine, which can be applied to wafer processing (**Jain**: Abstract; Pg. 372 Section V Dedicated MPE).

Further, **Sonderman & Jain teaches** ***providing*** *a first principles simulation result process* (**Sonderman**: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) *from the solution of the computer- encoded differential equations* (**Jain**: Abstract & Pg. 372 Section V Dedicated MPE) *and in accordance with the process data relating to the actual process being performed* (**Sonderman**: at least in Col.3 Lines 50-67; Col.7 Lines 8-20) *and* ***using*** *the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool* (**Sonderman**: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Arguendo, even if **Sonderman and Jain** do no explicitly teach said first principles simulation result being produced in a time frame shorter in time than the actual process being performed **Tan** teach the above limitation.

Tan *teaches said first principles simulation result being produced in a time frame shorter in time than the actual process being performed as in Col.2 Lines 7-12 as:*

(4) Model-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run, ensuring that product characteristics are achieved.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Jain** to **Sonderman** to solve differential equation for the semiconductor processing tool. **Sonderman** teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (**Sonderman**: Fig.1; Col.7 Lines 8-20), while **Jain** makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (**Jain**: Abstract).

*It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to facilitate the simulation as defined in Fig.2. The motivation to combine is that both **Tan** and **Sonderman** teach performing simulation of semiconductor assembly line including the tools and the processes running on them (**Tan**: Col.5 Line 63-Col.6 Line 8; **Sonderman**: **Sonderman**: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

Regarding Claim 38 (Updated 9/3/2010)

System claim 38 (**Sonderman**: Fig.1, **Tan**: 6-7) discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 75 (Updated 9/3/2010)

Apparatus claim 75 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (e.g. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (**Sonderman**: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (**Sonderman**: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-7, 9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (**Sonderman**: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20). **Sonderman** and **Jain** teach inputting fundamental equations as the set of computer encoded differential

equations (**Sonderman**: Col.9 (equations); **Jain**: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (**Sonderman**: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool (**Sonderman**: at least in Col.5-8; Fig.3-6 especially col.7).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (**Sonderman**: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (**Sonderman**: Semiconductor tools on the factory floor – Col.9 Lines 60-65) to perform first principle simulation (**Jain**: Section III); using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the

semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of subs**Tan**tially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (**Sonderman**: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (**Sonderman**: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 29

Sonderman teaches performing a principle components analysis to determine a relationship between spatial components of said first principles simulation result for the semiconductor processing tool and a set of at least one control variable, said relationship utilized to determine a correction to said set of at least one control variable in order to affect a reduction in the magnitude of said spatial components (**Sonderman**: Col.5 Line 56 – Col.6 Line 23).

Regarding Claim 30

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing

system for thermal annealing, and a batch diffusion furnace (**Sonderman**: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 32

Sonderman teaches inputting various parameters *as tool data* relating to etching, deposition etc. (**Sonderman**: at least in Col.5 Lines 56-67).

Regarding Claim 33

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (**Sonderman**: Col.5 Lines 56-67).

Regarding Claim 34

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (**Sonderman**: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 37

Sonderman teaches inspecting process results and providing input to the first principles simulation for calibration purposes (**Sonderman**: Col.6 Lines 14-24).

Regarding Claim 39

System claim 39 discloses similar limitations as claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 40-42

System claims 40-42 disclose similar limitations as claims 3-5 and are rejected for the same reasons as claims 3-5 respectively.

Regarding Claims 43-44, 46

System claims 43-46 disclose similar limitations as claims 6-9 and are rejected for the same reasons as claims 6-9 respectively.

Regarding Claim 47

System claim 47 discloses similar limitations as claim 10 and is rejected for the same reasons as claim 10.

Regarding Claim 48

System claims 48 disclose similar limitations as claim 11 and are rejected for the same reasons as claim 11 respectively.

Regarding Claim 51

System claim 51 discloses similar limitations as claim 14 and is rejected for the same reasons as claim 14.

Regarding Claims 52-56

System claims 52-56 disclose similar limitations as claims 15-19 and are rejected for the same reasons as claims 15-19 respectively.

Regarding Claims 57-58

System claims 57-58 disclose similar limitations as claims 20–21 and are rejected for the same reasons as claims 20-21 respectively. *Change in dependency from claim 52 to claim 38 of claim 57 is noted.*

Regarding Claim 66

System claim 66 discloses similar limitations as claim 29 and is rejected for the same reasons as claim 29.

Regarding Claim 67

System claim 67 discloses similar limitations as claim 30 and is rejected for the same reasons as claim 30.

Regarding Claim 69

System claim 69 discloses similar limitations as claim 32 and is rejected for the same reasons as claim 32.

Regarding Claim 70

System claim 70 discloses similar limitations as claim 33 and is rejected for the same reasons as claim 33.

Regarding Claim 71

System claim 71 discloses similar limitations as claim 34 and is rejected for the same reasons as claim 34.

Regarding Claim 74

System claim 74 discloses similar limitations as claim 37 and is rejected for the same reasons as claim 37.

Regarding Claims 79-80

Jain *teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (**Jain**: Pg. 367-368 Section*

"Governing Rationale" Sub-Section A. Governing Equations). ***Sonderman*** *also teaches initializing the models with input data (**Sonderman**: Col.7 Lines 8-20).*

15. Claims 22 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view Tan, further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).

Regarding Claim 22

Teachings of **Sonderman** and **Jain** are disclosed in claim 1 rejection above. **Sonderman** also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (**Sonderman**: at least in Col.5 Lines 62-67). **Jain** also teaches distributed and dedicated hardware implementation to solving wafer problem using computer implemented differential equations (**Jain**: Section III & IV).

Sonderman, **Jain** & **Tan** do not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code.

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

Motivation to combine **Jain with Sonderman** is disclosed above.

*It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to facilitate the simulation as defined in Fig.2. The motivation to combine is that both **Tan** and **Sonderman** teach performing simulation of semiconductor assembly line*

*including the tools and the processes running on them (**Tan**: Col.5 Line 63-Col.6 Line 8; **Sonderman**: **Sonderman**: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to **Sonderman** and **Jain** to create a equipment model as disclosed by **Sonderman**. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and **Sonderman** is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. Further, ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Motivation to combine **Jain** and Yunemura is that **Jain** as taught above indicates distributed solving of computer implemented differential equations which Yunemura solves by ANSYS modeling, thereby facilitating in implementation of **Jain**'s teachings.

Regarding Claim 59

System claim 59 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

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16. **Claims 23-28 and 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view of Tan, further in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter).**

Regarding Claims 23-25

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above.

Sonderman, **Jain** & **Tan** does not explicitly teach close fitting the solution of the first principle simulation run to thereby set the initial conditions for cells in the first principle simulation; selecting close fitting solutions from a library based on convergence.

Chen teaches close fitting the solution of the first principle simulation run to thereby set the initial conditions for cells in the first principle simulation (**Chen**: Col.6 Lines 26-38); selecting close fitting solutions from a library based on convergence (**Chen**: at least in Col.5 Lines 38 – Col.6 Line 25; Fig 3A-B, Fig.2; Col.4 Line 55 – Col.6 Line 19).

Motivation to combine **Jain** with **Sonderman** is disclosed above.

*It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Tan** to **Sonderman** to facilitate the simulation as defined in Fig.2. The motivation to combine is that both **Tan** and **Sonderman** teach performing simulation of semiconductor assembly line including the tools and the processes running on them (**Tan**: Col.5 Line 63-Col.6 Line 8; **Sonderman**: **Sonderman**: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig.1-3).*

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Chen** to **Sonderman** and **Jain**. The motivation to combine would have been that **Chen** and **Sonderman** both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (**Chen**: at least in Col.3 Lines 19-23).

Regarding Claim 26

Chen teaches that the close-fitting solution library existing on a network of computers connected to semiconductor-processing tool (**Chen**: Fig.2; Col.4 Line 55 –Col.6 Line 19).

Regarding Claims 27-28

Chen teaches calculating solution to the first principle simulation by choosing a coarse grid for solution to the first principle simulation (**Chen**: at least in Col.6 Line 44-Col.7 Line 14) as user defined parameters; further, subsequent solutions by setting the initial conditions to fine grid are made though Gaussian distribution and actual inline data (**Chen**: at least in Col.6 Line 46-51).

Regarding Claims 60-62

System claims 60-62 disclose similar limitations as claims 23-35 and are rejected for the same reasons as claims 23-25 respectively.

Regarding Claim 63

System claim 63 discloses similar limitations as claim 26 and is rejected for the same reasons as claim 26.

Regarding Claims 64-65

System claims 64-65 disclose similar limitations as claims 27-28 and are rejected for the same reasons as claims 27-28 respectively.

17. Claims 31, 36, 68 and 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain, further in view Tan, further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).

Regarding Claim 31

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above. **Sonderman** provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) but **Sonderman**, **Jain** & **Tan** do not explicitly disclose chemical vapor and physical vapor deposition system.

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (**Nikoonahad**: Col.24 Lines 3-49).

Motivation to combine **Jain** with **Sonderman** is disclosed above.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Nikoonahad** to **Sonderman** and **Jain**. The motivation to combine would have been that **Nikoonahad** and **Sonderman** are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (**Sonderman**: Abstract; **Nikoonahad**: Col.3; Col.93 Lines 20-35).

<u>Regarding Claim 36</u>

Nikoonahad teaches plurality of computing (as processor)/ storage (as memory) devices connected over network to exchange information between a plurality of computing/storage devices including at least one of model solver parameters, solution status to the first principles simulation, model solutions to the first principles simulation, and solution convergence history for said model solutions (**Nikoonahad**: Col.3 Lines 15-44; Col.68, Lines 41-59).

<u>Regarding Claim 68</u>

System claim 68 discloses similar limitations as claim 31 and is rejected for the same reasons as claim 31.

<u>Regarding Claim 73</u>

System claim 73 discloses similar limitations as claim 36 and is rejected for the same reasons as claim 36.

18. **Claims 35 and 72 are rejected under 35 U.S.C. 103(a) as being unpatentable over <u>Sonderman</u>, in view of <u>Jain</u>, further in view <u>Tan</u>, further in view of U.S. Application 10/472,436 filed by David Fatke et al. (<u>Fatke</u> hereafter).**

<u>Regarding Claim 35</u>

Teachings of **Sonderman**, **Jain** & **Tan** are disclosed in claim 1 rejection above.

Sonderman, **Jain** & **Tan** do not teach step of controlling by utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control.

Fatke teaches utilizing at least on of non-linear optimization and multivariate analysis to derive the control model for the process control (**Fatke**: [0011][0012][0035][0050]-[0058][0021]). **Fatke** uses the partial least square (PLS) model to perform multivariate analysis ([0050] to derive the control model for the process control and provide output to the semiconductor-processing tool ([0021]). Further, **Fatke** teaches that the nonlinear optimization is known in the art for creating such models ([0012]).

Motivation to combine **Jain** with **Sonderman** is disclosed above in claim 1.

Motivation to combine **Tan** with **Sonderman** is disclosed above in claim 1.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of **Fatke** to **Sonderman** and **Jain**. The motivation to combine would have been that **Fatke** and **Sonderman** are analogous art and **Fatke** creates a model form the determining the endpoint of the etching in an etch reactor (**Fatke**: Abstract/Summary), thereby creating a equipment model and the process model for etching, which can be applied to **Sonderman**.

Regarding Claim 72

System claim 72 discloses similar limitations as claim 35 and is rejected for the same reasons as claim 35. Motivation to combine **Jain** with **Sonderman** is disclosed above in claim 38. Motivation to combine **Tan** with **Sonderman** is disclosed above in claim 38.

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Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 8:00- 6:00 PM Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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